## **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

## **Listings of Claims:**

1. (currently amended) An NPN transistor formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the transistor comprising:

an N-type isolation <u>structure</u> <u>region</u> extending downward from a surface of the substrate, the N-type isolation <u>structure</u> <u>region</u> comprising a deep N layer and an annular N well, <u>the deep N layer overlapping the annular N well so as to enclose</u> <u>the N-type</u> <u>isolation region enclosing</u> an isolated P region of the <u>P-type</u> substrate, the N-type isolation <u>structure</u> <u>region</u> also forming a collector of the transistor, the isolated P region forming <u>at least a portion of</u> a base of the transistor;

wherein <u>a doping profile</u> in a vertical cross section of the N well <u>is non-monotonic</u> comprises a retrograde doping profile;

an N-type region located at the surface of the substrate within the isolated P region, the N-type region forming an emitter of the transistor;

a shallow P-type <u>base contact</u> region within the isolated P region to facilitate electrical contact to the base of the transistor, the shallow P-type <u>base contact</u> region having a doping concentration higher than <u>a doping concentration of</u> the substrate, and

electrical contacts to the emitter, the base and the collector in order to facilitate electrical biasing of the NPN transistor.

- 2. (new) The NPN transistor of claim 1 wherein the non-monotonic doping profile of the N well comprises multiple ion implantations of phosphorus at differing energies.
- 3. (new) The NPN transistor of claim 1 wherein the non-monotonic doping profile of the N well is non-Gaussian.

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blv
Suite 360
'anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

- 4. (new) The NPN transistor of claim 1 wherein a peak doping concentration of the deep N layer is located at a sufficient depth in the substrate such that a portion of the isolated P region located above the deep N layer is not counter-doped and converted to P-type material.
- 5. (new) The NPN transistor of claim 1 wherein the deep N layer comprises a high energy ion implantation of phosphorus.
- 6. (new) The NPN transistor of claim 1 wherein a junction breakdown voltage between the N-type region and the isolated P region is not limited by surface zener breakdown.
- 7. (new) The NPN transistor of claim 1 wherein a junction breakdown voltage between the N-type region and the isolated P region exceeds 6.5V.
- 8. (new) The NPN transistor of claim 1 wherein the N-type region and the shallow P-type base contact region do not touch or overlap.
- 9. (new) The NPN transistor of claim 1 wherein a junction breakdown voltage between the N-type region and the isolated P region is substantially the same as a junction breakdown voltage between the N-type isolation structure and the isolated P region.
- 10. (new) An NPN transistor formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the transistor comprising:

an N-type isolation structure extending downward from a surface of the substrate, the N-type isolation structure comprising a deep N layer and an annular N well, the deep N layer overlapping the annular N well so as to enclose an isolated P region of the substrate, the N-type isolation structure forming a collector of the transistor;

wherein a doping profile in a vertical cross section of the N well is non-monotonic; an implanted P base region located at the surface of the substrate within the isolated P region, the P base region and the isolated P region forming a base of the transistor, and

an N-type region located at the surface of the substrate within the P base region, the N-type region forming an emitter of the transistor; and

SILICON VALLEY
'ATENT GROUP LLP

50 Mission College Blvd
Suite 360
'anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

electrical contacts to the emitter, the base and the collector in order to facilitate the electrical biasing of the NPN transistor.

- 11. (new) The NPN transistor of claim 10 wherein the N well comprises multiple ion implantations of phosphorus at differing energies.
- 12. (new) The NPN transistor of claim 10 wherein the doping profile of the N well is non-Gaussian.
- 13. (new) The NPN transistor of claim 10 wherein a peak doping concentration of the deep N layer is located at a sufficient depth in the substrate such that a portion of the P base region located above the deep N layer is not counter-doped and converted to P-type material.
- 14. (new) The NPN transistor of claim 10 wherein the deep N layer comprises a high energy ion implantation of phosphorus.
- 15. (new) The NPN transistor of claim 10 wherein a junction breakdown voltage of the N-type region to the P base region is determined in part by a dopant concentration in the P base region.
- 16. (new) The NPN transistor of claim 10 wherein the P base region is formed by multiple ion implantations of differing energy.
- 17. (new) An NPN transistor formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the transistor comprising:

an N-type isolation structure extending downward from a surface of the substrate, the N-type isolation structure comprising a deep N layer and an annular N well, the deep N layer overlapping the annular N well so as to enclose an isolated P region of the P-type substrate, the N-type isolation structure also forming a collector of the transistor;

wherein a doping profile in a vertical cross section of the N well is non-monotonic; an implanted P well located at the surface of the substrate within the isolated P region, the P well and the isolated P region forming a base of the transistor;

an N-type region located at the surface of the substrate within the implanted P well, the N-type region forming an emitter of the transistor;

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blw
Suite 360
'anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

electrical contacts to the emitter, the base and the collector in order to facilitate electrical biasing of the NPN transistor.

- 18. (new) The NPN transistor of claim 17 wherein the annular N well comprises multiple ion implantations of phosphorus at differing energies.
- 19. (new) The NPN transistor of claim 17 wherein the doping profile of the N well is non-Gaussian.
- 20. (new) The NPN transistor of claim 17 wherein a peak doping concentration of the deep N layer is located at a sufficient depth such that a portion of the P well is not counter-doped and converted to N-type material.
- 21. (new) The NPN transistor of claim 17 wherein the deep N layer comprises a high energy ion implantation of phosphorus.
- 22. (new) The NPN transistor of claim 17 wherein a junction breakdown voltage of the N-type region to the base is determined by a doping concentration of the P well.
- 23. (new) The NPN transistor of claim 17 the P well comprises multiple ion implantations of differing energy.
- 24. (new) The NPN transistor of claim 17 wherein a doping profile in a vertical cross section of the P well is non-monotonic.
- 25. (new) The NPN transistor of claim 24 wherein the doping profile of the P well is non-Gaussian.
- 26. (new) The NPN transistor of claim 17 wherein a doping profile of the P well comprises a higher concentration portion and a lighter concentration portion, the lighter concentration portion being located closer to the surface of the substrate than the higher concentration portion.
- 27. (new) The NPN transistor of claim 17 wherein the P well is located atop the deep N layer.
- 28. (new) The NPN transistor of claim 27 wherein the P well comprises a higher concentration portion and a lighter concentration portion, the lighter concentration portion being located closer to the surface of the substrate than the higher concentration portion,

SILICON VALLEY
\*ATENT GROUP LLP
50 Mission College Blv
Suite 360
\*anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

and wherein a junction breakdown voltage of the P well relative to the deep N layer exceeds some specified base-to-collector breakdown voltage.

- 29. (new) The NPN transistor of claim 28 wherein the specified base-to-collector breakdown voltage is 5.5V.
- 30. (new) The NPN transistor of claim 28 wherein the specified base-to-collector breakdown voltage is 13.2V.
- 31. (new) The NPN transistor of claim 17 comprising a field oxide layer on the surface of the substrate, an opening being formed in the field oxide layer, the P well spanning the opening, the N-type region being located in the opening and being spaced apart from the field oxide region.
- 32. (new) The NPN transistor of claim 17 comprising a field oxide layer on the surface of the substrate, first and second openings being formed in the field oxide layer, the P well being electrically shorted to the surface of the substrate in the first opening, a junction between the N-type region and the P well extending across the second opening, the P well extending under the first and second openings and a section of the field oxide layer between the first and second openings.
- 33. (new) The NPN transistor of claim 32 including a P-type base contact region located within the P well and at the surface of the substrate in the first opening, the P-type base contact region having a doping concentration higher than a doping concentration of the P well.
- 34. (new) A PNP transistor formed in a semiconductor substrate, the substrate being doped with P-type impurity and not comprising an epitaxial layer, the transistor comprising:

an N-type isolation structure extending downward from a surface of the substrate, the N-type isolation structure comprising a deep N layer and an annular N well, the deep N layer overlapping the annular N well so as to enclose an isolated P region of the P-type substrate:

the isolated P region containing:

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blvd
Suite 360
'anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

an implanted P well adjacent the surface of the substrate, the P well forming a collector of the transistor, wherein a doping profile in a vertical cross section of the P well is non-monotonic;

an N-type base region located adjacent the surface within the P well, the N-type base region forming a base of the transistor; and

a P-type region located adjacent the surface within the N-type base region, the P-type region forming an emitter of the transistor; and

electrical contacts to the emitter, the base, and the collector in order to facilitate electrical biasing of the PNP transistor, and an additional electrical contact to the N-type isolation structure to facilitate biasing of the N-type isolation structure relative to a portion of the substrate surrounding the N isolation structure.

- 35. (new) The PNP transistor of claim 34 wherein a doping profile in a vertical cross section of the N well is non-monotonic.
- 36. (new) The PNP transistor of claim 34 wherein the non-monotonic doping profile of the N well comprises multiple ion implantations of phosphorus at differing energies.
- 37. (new) The PNP transistor of claim 34 wherein the non-monotonic doping profile of the N well is non-Gaussian.
- 38. (new) The PNP transistor of claim 34 wherein the substrate has a background doping concentration and wherein a peak doping concentration of the deep N layer is located at a sufficient depth such that a portion of the substrate with the background doping concentration remains above the deep N layer and below the P well.
- 39. (new) The PNP transistor of claim 34 wherein a junction breakdown voltage of the P well to the deep N layer is greater than a specified minimum collector to isolation voltage.
- 40. (new) The PNP transistor of claim 34 wherein the deep N layer comprises a high energy ion implantation of phosphorus.
- 41. (new) The PNP transistor of claim 34 wherein the non-monotonic doping profile of the P well comprises multiple ion implantations of boron at differing energies.

SILICON VALLEY
ATENT GROUP LLP
50 Mission College Blvd
Suite 360
ianta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

- 42. (new) The PNP transistor of claim 34 wherein the non-monotonic doping profile of the P well is non-Gaussian.
- 43. (new) A PNP transistor formed in a semiconductor substrate and not comprising an epitaxial layer, the substrate being doped with P-type impurity, the transistor comprising:

an N-type isolation structure extending downward from a surface of the substrate, the N-type isolation structure comprising a deep N layer and an annular N well, the deep N layer overlapping the annular N well so as to enclose an isolated P region of the P-type substrate;

a field oxide layer at a portion of the surface of the substrate above the isolated P region, at least first and second openings being formed in the field oxide layer,

the isolated P region containing:

an implanted P well adjacent the surface of the substrate, the P well forming a collector of the transistor, wherein a doping profile in a vertical cross section of the P well is non-monotonic;

an N-type base region located within the P well, the N-type base region forming a base of the transistor; and

a P-type region, the P-type region forming an emitter of the transistor;

the N-type base region being electrically contacted in the first opening, the P-type region having a junction with the N-type base region, the junction extending across the second opening, the N-type base region extending under the first and second openings and a section of the field oxide layer between the first and second openings; and

electrical contacts to the emitter, the base, and the collector in order to facilitate electrical biasing of the PNP transistor, and an additional electrical contact to the N-type isolation structure to facilitate biasing of the N-type isolation structure relative to a portion of the substrate surrounding the N-type isolation structure.

44. (new) The PNP transistor of claim 43 comprising a N-type base contact region within the N-type base region, the N-type base contact region being located at the

SILICON VALLEY
\*ATENT GROUP LLP
50 Mission College Blv
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

surface of the substrate in the first opening and having doping concentration higher than a doping concentration of the N-type base region.

- 45. (new) The PNP transistor of claim 43 wherein a doping profile in a vertical cross section of the N well is non-monotonic, the N well comprising multiple ion implantations of phosphorus at differing energies.
- 46. (new) The PNP transistor of claim 43 wherein the non-monotonic doping profile of the N well is non-Gaussian.
- 47. (new) The PNP transistor of claim 43 where the substrate has a background doping concentration and wherein a peak doping concentration of the deep N layer is located at a sufficient depth such that a portion of the substrate with the background doping concentration remains above the deep N layer and below the P well.
- 48. (new) The PNP transistor of claim 43 wherein a junction breakdown voltage of the P well to the deep N layer is greater than a specified collector to isolation voltage.
- 49. (new) The PNP transistor of claim 43 wherein the deep N layer comprises a high energy ion implantation of phosphorus.
- 50. (new) The PNP transistor of claim 43 wherein the non-monotonic doping profile of the P well comprises multiple ion implantations of boron at differing energies.
- 51. (new) The PNP transistor of claim 43 where the non-monotonic doping profile of P well is non-Gaussian.
- 52. (new) The PNP transistor of claim 43 where the N base comprises a series of phosphorus ion implantations of differing energy.
- 53. (new) A complementary pair of isolated bipolar transistors formed in a P-type substrate, the substrate not comprising an epitaxial layer, the complementary pair of isolated bipolar transistors comprising:

a plurality of N-type isolation structures, each of the isolation structures extending downward from a surface of the substrate and comprising a deep N layer and an annular N well, the deep N layer overlapping the annular N well so as to enclose an isolated region of

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blv
Suite 360
ianta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

the substrate, each of the N-type isolation structures serving to isolate one of the isolated bipolar transistors from a region of the substrate outside of the N-type isolation structure; an NPN transistor comprising:

a first one of the N-type isolation structures enclosing a first isolated P region of the P-type substrate, the first one of the N-type isolation structures forming a collector of the NPN transistor and providing electrical isolation of the NPN transistor from a region of the substrate outside of the first one of the N-type isolation structures, the first isolated P region containing:

a first P well located at the surface of the substrate within the first isolated P region, the first P well having a doping concentration higher than a doping concentration of the P-type substrate, the first P well and the first isolated P region forming the base of the NPN transistor; and

an N-type region located at the surface of the substrate within the P well, the N-type region forming the emitter of the transistor; and a PNP transistor comprising:

a second one of the N-type isolation structures enclosing a second isolated P region of the P-type substrate and providing electrical isolation of the PNP transistor from a region of the substrate outside of the second one of the N-type isolation structures, the second isolated P region containing:

a second implanted P well adjacent the surface of the substrate, the second isolated P region and the second P well forming a collector of the PNP transistor;

an N-type base region located adjacent the surface within the second P well, the N-type base region forming a base of the PNP transistor; and a P-type region located adjacent the surface within the N-type base region, the P-type region forming an emitter of the PNP transistor.

54. (new) The complementary pair of bipolar transistors of claim 53 wherein respective doping profiles taken through vertical cross sections of the first P well and second P well are the same.

SILICON VALLEY 'ATENT GROUP LLP

50 Mission College Blvd Suite 360 Santa Clara, CA 95054 (408) 982-8200 FAX (408) 982-8210

- 55. (new) The complementary pair of bipolar transistors of claim 54 wherein the respective doping profiles taken through vertical cross sections of the first P well and the second P well are non-monotonic.
- 56. (new) The complementary pair of bipolar transistors of claim 55 wherein the non-monotonic doping profiles of the first and second P wells comprise multiple ion implantations of boron at differing energies.
- 57. (new) The complementary pair of bipolar transistors of claim 55 wherein the non-monotonic doping profiles of the first and second P wells are non-Gaussian.
- 58. (new) The complementary pair of bipolar transistors of claim 54 wherein the first and second P wells have a peak doping concentration at a greater depth and a lighter doping concentration at a shallower depth, so as to minimize the counter doping of the N-type region in the NPN transistor and the N-type base region in the PNP transistor.
- 59. (new) The complementary pair of bipolar transistors of claim 54 wherein a thickness of the first P well primarily determines the bipolar current gain of the NPN transistor.
- 60. (new) The complementary pair of bipolar transistors of claim 53 wherein each of the deep N layers is formed by a high energy ion implantation of phosphorus.
- 61. (new) The complementary pair of bipolar transistors of claim 53 wherein the substrate has a background doping concentration and wherein each of the deep N layers is located at a sufficient depth such that a portion of the substrate with the background doping concentration is located above the deep N layer and below the P well.
- 62. (new) The complementary pair of bipolar transistors of claim 53 wherein a junction breakdown voltage of each of the first P well and second P well with respect to the deep N layer in the isolation structure enclosing the P well exceeds a specified minimum voltage.
- 63. (new) The complementary pair of bipolar transistors of claim 53 wherein a doping profile of the annular N well in each of the N-type isolation structures is non-monotonic.

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blv
Suite 360
'anna Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

- 64. (new) The complementary pair of bipolar transistors of claim 63 wherein the doping profile of the annular N well in each of the N-type isolation structures comprises multiple ion implantations of phosphorus at differing energies.
- 65. (new) The complementary pair of bipolar transistors of claim 63 wherein the doping profile of the annular N well in each of the N-type isolation structures is non-Gaussian.
- 66. (new) The complementary pair of bipolar transistors of claim 53 wherein the doping profile of the annular N well in each of the N-type isolation structures is electrically shorted to the deep N layer in the same N-type isolation structure.
- 67. (new) The complementary pair of bipolar transistors of claim 53 further comprising:

a field oxide layer on the surface of the substrate, the field oxide layer having at least first and second openings formed therein;

the first one of the N-type isolation structures reaching the surface at a location underneath the field oxide layer, the first P well spanning the first opening, the N-type region being located in the first opening and being spaced apart from the field oxide region; and

the second one of the N-type isolation structures reaching the surface at a location underneath the field oxide layer, the second P well spanning the second opening, the N-type base region being located in the second opening and being spaced apart from the field oxide region.

- 68. (new) The complementary pair of bipolar transistors of claim 53 further comprising:
- a field oxide layer on the surface of the substrate, the field oxide layer having at least first, second, third and fourth openings formed therein;

the first P well reaching the surface of the substrate in the first opening, the N-type region having a junction with the P well, the junction extending across the second opening, the first P well extending under the first and second openings as well as a section of the field oxide layer between the first and second openings; and

SILICON VALLEY
'ATENT GROUP ILP
50 Mission College Blve
Suite 360
'anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

the N-type base region reaching the surface of the substrate in the third opening, the P-type region having a junction with the N-type base region, the junction extending across the fourth opening, the N-type base region extending under the third and fourth openings as well as a section of the field oxide layer between the third and fourth openings.

- 69. (new) The complementary pair of bipolar transistors of claim 53 further comprising a P base contact region within the first P well, the P base contact region having a doping concentration higher than a doping concentration of the first P well and being located adjacent the surface of the substrate in the first opening.
- 70. (new) The complementary pair of bipolar transistors of claim 53 further comprising an N base contact region within the N-type base region, the N base contact region having a doping concentration higher than a doping concentration of the N-type base region and being located adjacent the surface of the substrate in the third opening.